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Stacking Voltage-Controlled Oscillators: Analysis and Application.

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Stacking Voltage-Controlled Oscillators: Analysis and Application

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***Abstract*—The paper proposes a method to regulate the output frequency and duty cycle (phase) of ring oscillator by emulating a resistive voltage divider using purely digital means. To this end an additional master oscillator that can be pulsed by an external frequency is connected in series with a slave one. Since the inherent frequency of ring oscillator depends on its supply voltage, the behavioral model of the system is a stack of voltage-controlled oscillators. The paper derives an analytical expression for the slave frequency as a function of the master frequency and the impedance of the switching circuitry loading the master. The obtained theory agrees well with the results of simulations.**

Keywords—equivalent resistance, frequency mirror, impedance, nonlinear circuits, pulse width modulation, switched capacitor.

I. Introduction

In the vast majority of digital circuits, voltage controlled oscillators (VCOs) are built using ring oscillators. The dependence of the VCO output frequency on the controlling voltage can be linear or non-linear. Linear VCOs use voltage controlled current source built on the MOS transistor operating in the saturation mode. In nonlinear VCOs a voltage controlled resistance is used. Actually, this is the same transistor not entering saturation. In our proposed approach the controlled resistance is represented by impedance (equivalent resistance) between the power terminals of a ring oscillator. Such an impedance has been considered firstly in [1], [2].

It should be noted that the modulation of impedance leads to parametric excitation in all types of oscillators, including mechanical ones [3]. Recently, interest to parametric excitation is resumed in light of changing the traditional approaches to computing. For example, the phenomenon of sub-harmonic injection locking in oscillators is used in [4] to realize non-standard logic gates. An application of coupled oscillators to building associative memory is presented in [5]. In our circuit the current flowing through one oscillator defines how fast will operate the other. Thus, we emulate a self-adjusting voltage divider, where the impedances are reciprocal to the switching activity. If one of the oscillators slows down, it forces the other to run slower.

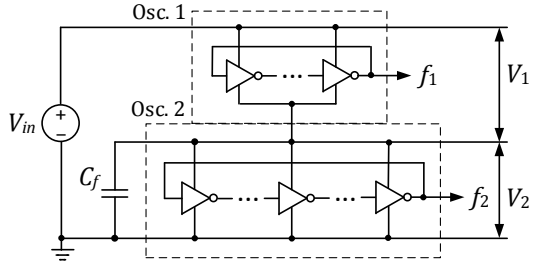


Fig. 1: Stack connection of two ring oscillators of different length.

The main effects taking place in the proposed circuit are:

1) transient, caused by the frequency change and followed by stabilization via the internal feedback "voltage–frequency–impedance–voltage".
2) steady state with some ripple, whose level depends on how the oscillators interact and on how well the products of this interaction are averaged.

The proposed method of stacking VCOs has been used to build a new type of frequency controlled pulse width modulation (PWM) circuit. Furthermore, this approach to modelling digital circuits as non-linear impedances allows building novel computing elements where the information carrier is duty cycle.

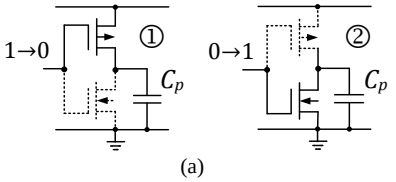
II. Proposed Approach

Let us consider a stack of two ring oscillators with different number of inverters shown in Fig. 1, where C_f is a filter (averaging) capacitor. To analyze it, we use the model of inverter presented in Fig. 2(a). This model is a simplified version of the model from [6] and does not take into account the parasitic effects such as short circuit current and leakage. The operation of the ring oscillator is represented in [1] as the switching between three states shown in Fig. 2(b). It should be noted that the switching of adjacent inverters, and consequently, recharging of the capacitors partly overlap. This effect is also ignored. The capacitance of $C_t = C_p\,(n-1)/2$ increases with increase of the number of inverters, n, but C_p does not depend on n and continuously recharges.

In a distinctive super-threshold region the propagation delay of an inverter is given as [7]:

$$t_{su} = \frac{pC_pV_{dd}}{(V_{dd}-V_{th})^{\alpha}} \qquad (1)$$

where $V_{th} < V_{dd}$ is the threshold voltage, $1.2 \le \alpha \le 2$ is the technology dependent parameter, and p is a fitting parameter. It can be shown that the ratio V_1/V_2 in Fig. 1 is equal to one and does not depend on the number of inverters. It is important to emphasize that we are talking about DC voltages, i.e. about average values of voltages in steady state. To pulse the ring oscillator with an external frequency, f_s, we use the Muller C-element [8] as shown in Fig. 3(a). For two inputs x_1 and x_2 the output of the C-element is given as $y = x_1x_2 + (x_1 + x_2)y$.



(a)

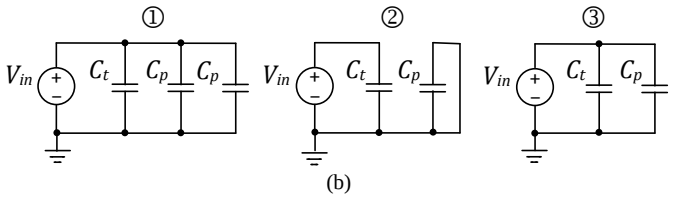


Fig. 2: Model of an inverter (a) and states of the ring oscillator (b).

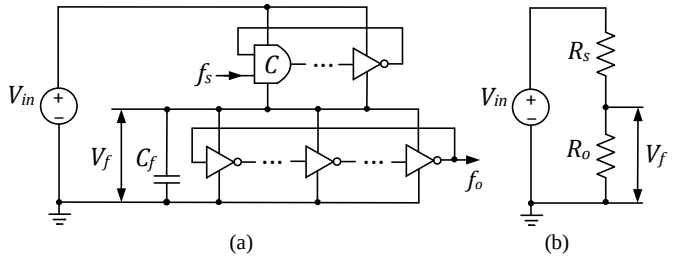


Fig. 3: Externally pulsed stack (a) and its equivalent circuit (b).

Thus, the stack can be considered as switched capacitors, which allows us to move to the equivalent circuit shown in Fig. 3(b). Assuming the C-element can be represented by a pair of inverters and all the inverters are identical,

$$R_s = \frac{1}{f_s C_p}; \quad R_o = \frac{1}{f_o C_p}; \quad \frac{V_f}{V_{in} - V_f} = \frac{R_o}{R_s} = \frac{f_s}{f_o} \tag{2}$$

As soon as the external frequency f_s is changed, the negative feedback starts to operate. First, the voltage V_2 is changing, which will change the output frequency f_o. This will lead to change in impedance R_2, which in turn, will correct V_2. Thus, after some transient the system will reach steady-state defined by (2). This can be explained by the fact that our system is self-adjusting and tends to minimize power dissipation. The behavioral model of the synchronized stack is similar to the model given in [2], with the exception of C-element as shown in Fig. 4.

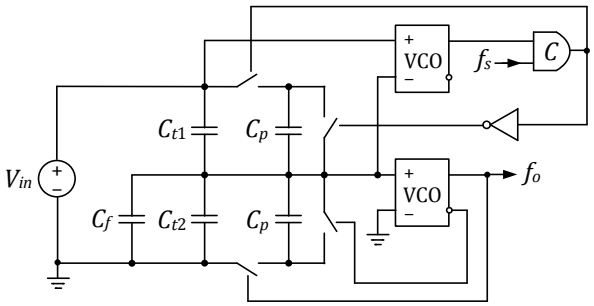


Fig. 4: Behavioral model of the pulsed stack.

The voltages in the stack can also be adjusted by an external switching activity. For this purpose, we shunt the oscillator with a binary tree of inverters as shown in Fig. 5(a).

In the case close to ideal, we can assume that all the inverters of the same level switch simultaneously. The equivalent circuit for this case is shown in Fig. 5(b). As before,

$$R_1 = \frac{1}{f_o C_p}; \quad R_2 = \frac{1}{f_s C_p}; \quad R_3 = \frac{1}{f_s C_L} \tag{3}$$

where $C_L = (2^d - 1)C_p$ is total capacitance of the tree defined by its depth d.

$$\frac{V_f}{V_{in} - V_f} = \frac{R_2 || R_3}{R_1} = \frac{f_o C_p}{f_s (C_p + C_L)} \tag{4}$$

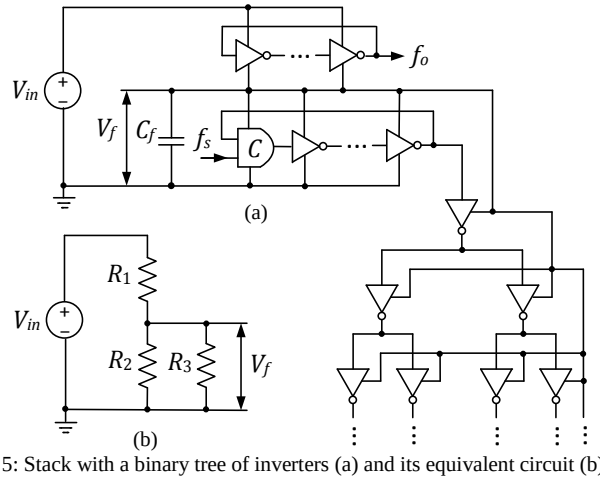


Fig. 5: Stack with a binary tree of inverters (a) and its equivalent circuit (b).

In general case the switching of the inverters from the apex towards the base of the tree can demonstrate effect similar to the interference in the wave propagation.

Cascading the synchronized stacks as shown in Fig. 6, we can decouple the control frequency from the ground. Such a cascade can be considered as a "frequency mirror", which generalises (2).

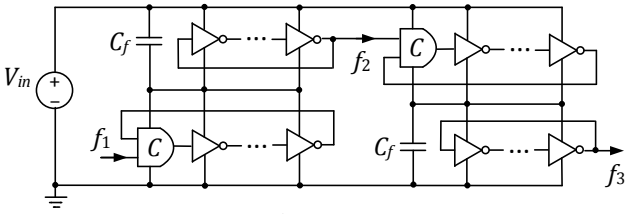


Fig. 6: Cascade of two synchronized stacks.

III. Application

The synchronized stack can be used for building a frequency controlled PWM circuit as shown in Fig. 7. Since we control the impedances, the transfer characteristic of the circuit will be nonlinear. A more or less linear PWM circuit of such type has been proposed in [9] and operates in the current mode. Let the initial state of the PWM output in Fig. 7 be logical "1" then:

$$t_{on} = (n-1)t_{su2}; \quad t_{off} = (n+1)t_{su1} \tag{5}$$

where t_{su1} and t_{su2} are the propagation delays of the inverter in odd and even positions, respectively. Letting in (1) $\alpha = 2$ and $V_{th} \ll V_{dd}$, we obtain $t_{su} \approx k/V_{dd}$, where k is some constant. Thus, the output frequency $f_o = 1/(t_{on} + t_{off})$ and duty cycle $D = t_{on} f_o$ are written as:

$$f_o = \frac{V_1 V_2}{k[(n-1)V_1 + (n+1)V_2]}$$
$$D = \frac{(n-1)V_1}{(n-1)V_1 + (n+1)V_2} \tag{6}$$

It is evident that f_o depends on $k = V_{dd} t_{su}$, which should be found experimentally. It should be noted that in the regular case when $V_1 = V_2$ the duty cycle $D = (n-1)/2n$ and tends to 0.5 for $n \to \infty$. The condition of $V_1 = V_2$ also allows us to use the relations (2) for the circuit in Fig. 7 as follows.

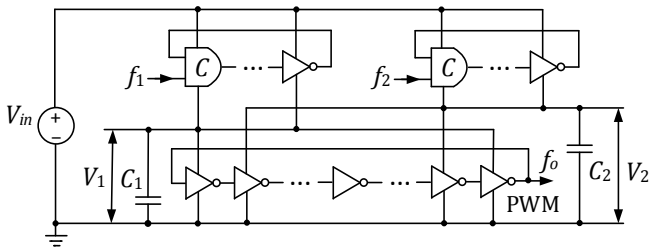


Fig. 7: Frequency controlled PWM circuit.

$$\frac{V_1}{V_{in}-V_1}=\frac{V_2}{V_{in}-V_2}=\frac{f_s}{f_o};\quad f_s=\frac{2nf_1}{n+1}=\frac{2nf_2}{n-1} \tag{7}$$

such that:

$$V_1=\frac{2nf_1V_{in}}{2nf_1+(n+1)f_o};\quad V_2=\frac{2nf_2V_{in}}{2nf_2+(n-1)f_o} \tag{8}$$

Substituting (8) into (6), we obtain:

$$\begin{gathered} f_o=\frac{2nf_1f_2V_{in}}{k([(n-1)^2f_1+(n+1)^2f_2]f_o+4n^2f_1f_2)} \\ D=\frac{(n-1)^2f_1f_o+2n(n-1)f_1f_2}{[(n-1)^2f_1+(n+1)^2f_2]f_o+4n^2f_1f_2} \end{gathered} \tag{9}$$

Thus, the output frequency is defined by a quadratic equation:

$$\begin{gathered} f_o^2+pf_o-q=0 \\ p=\frac{4n^2f_1f_2}{(n-1)^2f_1+(n+1)^2f_2} \\ q=\frac{2nf_1f_2V_{in}}{k[(n-1)^2f_1+(n+1)^2f_2]} \end{gathered} \tag{10}$$

The disadvantage of the PWM circuits of the considered type is that for different duty cycles the output frequency varies [9]. To solve this problem, we let f_o in (9) to be constant and express one control frequency through the other.

$$\begin{gathered} f_2(f_1)=\frac{k(n-1)^2f_o^2f_1}{2n(V_{in}-2knf_o)f_1-k(n+1)^2f_o^2} \\ D(f_1)=\frac{2n(V_{in}-(n+1)kf_o)f_1-(n+1)^2f_o^2}{2n(V_{in}-2kf_o)f_1-2(n+1)kf_o^2} \end{gathered} \tag{11}$$

The plots of these functions for $f_o=50k$Hz are presented in Fig. 8 in the logarithmic scale. As evident, with the increase of control frequency, function $D(f_1)$ rapidly loses sensitivity. The behavioral model of the frequency controlled PWM circuit is shown in Fig. 9 and resembles that of [10].

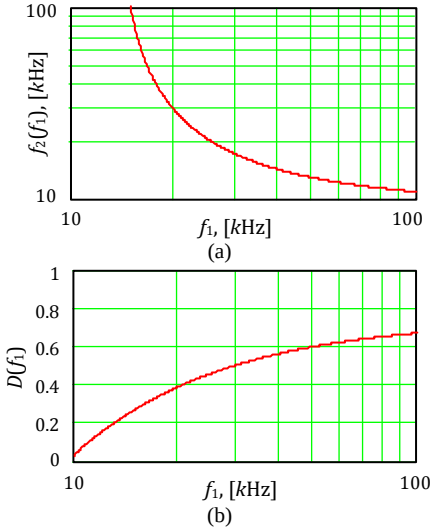


Fig. 8: Second control frequency f_2 as a function of the first one f_1 for the constant $f_o=50k$Hz (a) and duty cycle to which this dependence leads (b).

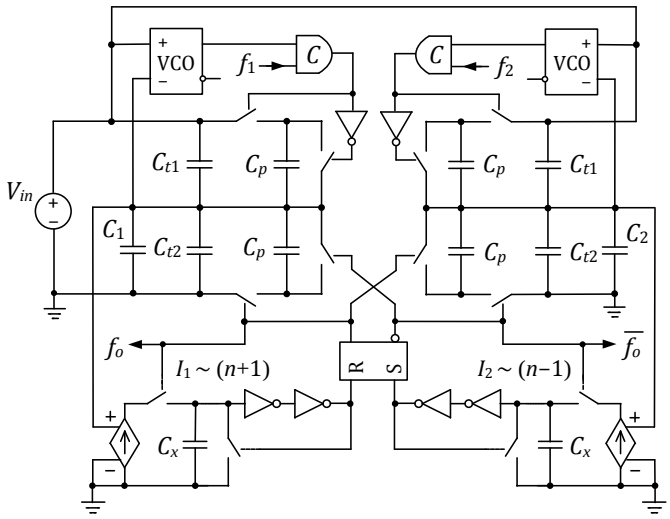


Fig. 9: Behavioral model of the frequency controlled PWM circuit.

IV. Simulation Results

To verify the above analytical results by simulation, we need to provide $\alpha=2$. This requirement is fulfilled well by the standard digital ICs. We used 74LVC04 low-voltage CMOS inverter, whose SPICE model was downloaded from the NXP site. The transistors taken from this model were used for building the inverters and C-elements. To provide high switching speed, we used the so-called static C-element built on 12 transistors [11]. Each of the C-elements is connected to one inverter, while the footer consists of $n=11$ inverters. The simulations have been carried out in SIMetrix Intro 8.0. The voltage $V_{in}=9V$, while $C_1=C_2=0.1\mu$F. Fig. 10 shows how the voltages in the circuit in Fig. 7 are settling for $f_1=64k$Hz and $f_2=32k$Hz.

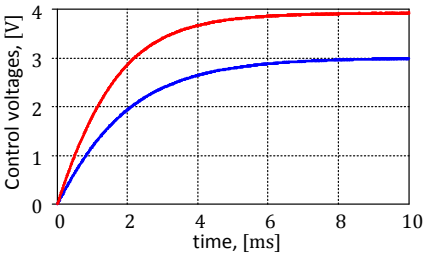


Fig. 10: Stabilization of the voltages for $f_1=64k$Hz and $f_2=32k$Hz with $C_1=C_2=0.1\mu$F. Upper trace: $V_1(t)$, bottom trace: $V_2(t)$.

Solid lines in Fig. 11 and Fig. 12 show f_o and D measured for the case of $f_1=f_2$. To find analytic values of f_o and D, we need first to determine k. Substituting $f_1=f_2=f$ into (10), we get:

$$k=\frac{V_{in}}{\left[\left(n+\frac{1}{n}\right)\frac{f_o}{f}+2n\right]f_o} \tag{12}$$

where f_o is taken from the previous measurements. Fig. 12 shows the plot of k calculated by (12). Since k is not constant, we need to choose some operating point. It is convenient to let $f_o=50k$Hz, which corresponds to $k=3.9\times10^{-6}$. The values of f_o and D measured for different f_1 and f_2 are presented in Fig. 14 and Fig. 15 respectively.

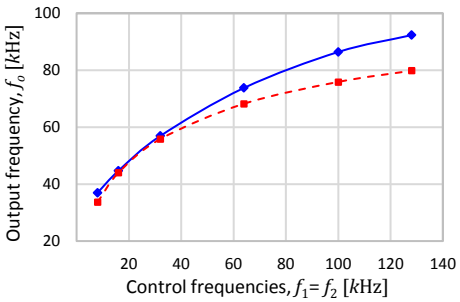


Fig. 11: Output frequency as a function of equal frequencies. Solid line: measured. Dashed line: calculated by (10).

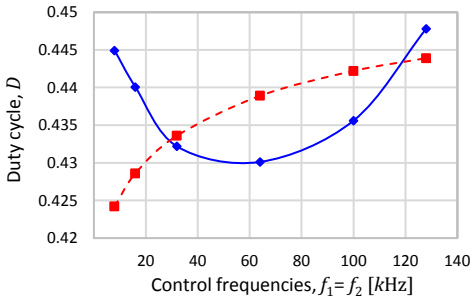


Fig. 12: Duty cycle as a function of two equal frequencies. Solid line: measured. Dashed line: calculated by (9).

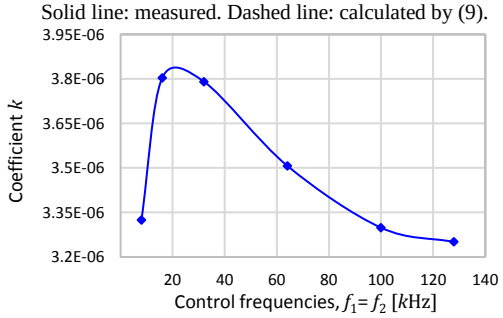


Fig. 13: Coefficient k as a function of two equal frequencies.

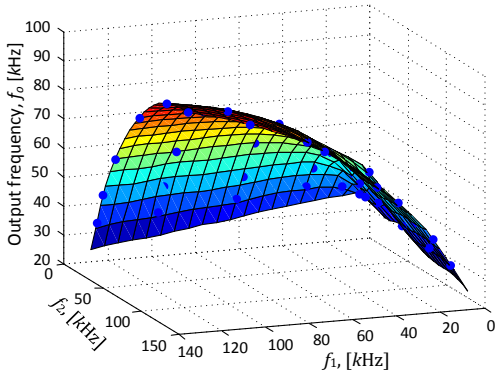


Fig. 14: Output frequency as a function of two control frequencies.

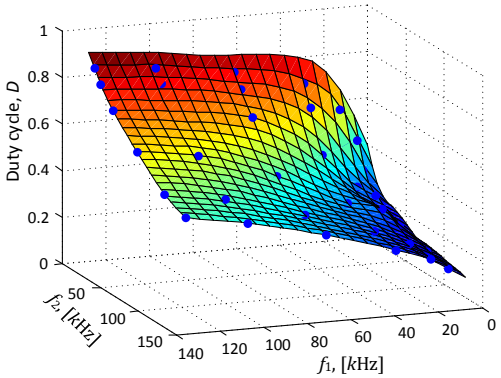


Fig. 15: Duty cycle as a function of two control frequencies.

V. Conclusions and Discussion

It has been shown that the stack of two ring oscillators represents a self-adjusting system, which is described well by impedances. The impedances of the stack can be controlled by the external frequency pulsing one of the oscillators. This feature has been used for building the frequency controlled PWM circuit. The output frequency of this circuit varies for different duty cycles. To keep it constant we expressed one control frequency through the other.

It should be noted that at very high control frequencies the C-elements might not have enough time to switch fully. On the contrary, at very low control frequency the low voltage drop across the footer will cause a similar problem with the inverters. This is because for very low V_{dd} the inverters enter the subthreshold region, where $\alpha \neq 2$. Thus, it would be advantageous to have inverting elements with delay strictly reciprocal to V_{dd}. Nevertheless, the discrepancy between the measured and calculated plots in Fig. 11 and Fig. 12 is small enough at the frequencies corresponding to the chosen operating point of $f_o = 50k\text{Hz}$.

In this work the interaction between oscillators was restricted to the ratios of their impedances, for which we used filter capacitances. On the other hand, quite contrary, one might exploit stronger types of interactions to perform oscillator-based computing, such as in [13], [14], [15].

An interesting direction is also development of frequency insensitive computational elements. That is such elements, where the information is represented by duty cycle (phase) and can be processed irrespectively of the carrier frequency. These elements, probably, will be able to operate correctly with big changes of the power supply voltage. To obtain frequency insensitive behavior we need to understand first how to keep D constant with different f_1 and f_2. Graphically, this means to consider a cross-section of the plot in Fig. 15 by Z-axis.

Acknowledgment

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